AMENDMENTS TO THE CLAIMS:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of Claims:

1. (Currently Amended) [[A]] The single electron transistor as claimed in claim 6 ~~having a memory function~~, further comprising:

~~a first substrate;~~

~~an insulation film stacked on the first substrate;~~

~~a second substrate stacked on the insulation film and including a source region, a channel region, and a drain region;~~

a tunneling film formed ~~on the second~~ between the substrate and the trap sections;

~~at least two trap layers formed on the tunneling film and separated by an interval such that at least one quantum dot can be formed in a same interval in the channel region; and~~

~~a gate electrode contacting the at least two trap layers and the tunneling film between the at least two trap layers~~.

2. (Currently Amended) The single electron transistor as claimed in claim 1, wherein the gate electrode extends on the at least two trap sections ~~layers~~.

3. (Currently Amended) The single electron transistor as claimed in claim 1, wherein ~~the insulation film and~~ the tunneling film is a ~~are~~ silicon oxide film ~~films~~.

4. (Original) The single electron transistor as claimed in claim 1, wherein a size of the at least one quantum dot is 100 nm or less at room temperature.

5. (Currently Amended) The single electron transistor as claimed in claim 1, wherein the at least two trap sections ~~layers~~ are a nitride ~~layers~~ or a ferro-dielectric ~~layers~~ including PZT ~~layers~~.

6. (Currently Amended) [[A]] The single electron transistor as claimed in claim 44, wherein ~~having a memory function, comprising:~~

~~a first substrate;~~

~~a first insulation film stacked on the first substrate;~~

~~a second substrate stacked on the first insulation film and including a source region, a channel region, and a drain region;~~

~~a second insulation film formed on the second substrate;~~

the trap layer includes at least two trap sections ~~layers included in the second insulation film and~~ separated by [[an]] the interval ~~such that at least one quantum dot can be formed in a same interval in the channel region, wherein electrons passing through the channel region are trapped in the at least two trap layers; and~~

~~a gate electrode formed on the second insulation film~~.

7. (Currently Amended) The single electron transistor as claimed in claim 6, wherein the at least two trap sections ~~layers~~ are a nitride ~~layers~~ or a ferro-dielectric ~~layers~~.

8. (Currently Amended) The single electron transistor as claimed in claim 6, further comprising an insulation film covering ~~wherein~~ the at least two trap sections ~~layers are completely covered with the second insulation film~~.

9. (Currently Amended) The single electron transistor as claimed in claim 8, wherein the at least two trap sections ~~layers~~ are sections ~~layers~~ selected from the group consisting of conductive material layers including a conductive silicon layer and a conductive germanium layer.

10. (Currently Amended) The single electron transistor as claimed in claim [[6]] 8, wherein ~~both~~ the ~~first and second~~ insulation ~~films are~~ film is an oxide film ~~films~~.

11. (Currently Amended) The single electron transistor as claimed in claim 6, wherein a size of the at least one quantum dot is 100 nm or less at room temperature.

12. (Currently Amended) [[A]] The single electron transistor as claimed in claim 44, wherein~~, comprising:~~

~~a first substrate;~~

~~a first insulation film stacked on the first substrate;~~

~~a second substrate stacked on the first insulation film and including a source region, a channel region, and a drain region;~~

~~a second insulation film formed on the second substrate;~~

~~a trap layer continuously formed on the second insulation film;~~

~~a third insulation film formed on the trap layer;~~

~~at least two fourth insulation film patterns formed on the third insulation film and having conductive spacers formed on facing ends thereof, wherein~~ the gate electrode includes conductive spacers [[are]] separated by [[an]] the interval ~~such that at least one quantum dot can be formed in a same interval in the channel region;~~

~~a fifth insulation film formed on and between the at least two fourth insulation film patterns having the conductive spacers formed thereon; and~~

~~a gate electrode formed on the fifth insulation film~~.

13. (Canceled).

14. (Original) The single electron transistor as claimed in claim 12, wherein the conductive spacers are silicon spacers.

15. (Original) The single electron transistor as claimed in claim 12, wherein a size of the at least one quantum dot is 100 nm or less at room temperature.

16. (Original) The single electron transistor as claimed in claim 12, wherein the trap layer is a nitride layer or a ferro-dielectric layer.

17. (Currently Amended) The single electron transistor as claimed in claim 12, further comprising an insulation film formed between the trap layer and the substrate, wherein ~~each of the second insulation film,~~ the trap layer and the ~~third~~ insulation film have a same thickness.

18. (Currently Amended) The single electron transistor as claimed in claim [[13]] 55, wherein a thickness of the another ~~fifth~~ insulation film is greater than ~~a thickness of the second insulation film and~~ a thickness of the ~~third~~ insulation film.

19. (Currently Amended) [[A]] The single electron transistor as claimed in claim 6, further comprising:

~~a first substrate;~~

~~a first insulation film stacked on the first substrate;~~

~~a second substrate stacked on the first insulation film and including a source region, a channel region, and a drain region;~~

~~a second insulation film formed on the second substrate;~~

~~at least two trap layer patterns having a separation distance therebetween formed on the second insulation film and in a third insulation film such that the third~~ an insulation film on and between ~~surrounds~~ the at least two trap sections ~~layer patterns on all surfaces except bottom surfaces thereof which contact the second insulation film;~~

~~at least two fourth insulation film patterns formed on the third insulation film and having conductive spacers formed on facing ends thereof, wherein the conductive spacers are formed to be in alignment with the at least two trap layer patterns and to be separated from each other by an interval such that at least one quantum dot can be formed in a same interval in the channel region, wherein the interval corresponds to the separation distance between the at least two trap layer patterns;~~

~~a fifth insulation film formed on and between the at least two fourth insulation film patterns having the conductive spacers formed thereon; and~~

~~a gate electrode formed on the fifth insulation film~~.

20. (Currently Amended) The single electron transistor as claimed in claim 19, wherein the at least two trap sections ~~layer patterns~~ are formed of a material selected from the group consisting of conductive materials including conductive silicon and conductive germanium.

21. (Currently Amended) The single electron transistor as claimed in claim 19, wherein the at least two trap sections ~~layer patterns~~ are formed of a nitride or a ferro-dielectric.

22. (Currently Amended) [[A]] The single electron transistor as claimed in claim 44, further comprising:

~~a first substrate;~~

~~a first insulation film stacked on the first substrate;~~

~~a second substrate stacked on the first insulation film and including a source region, a channel region, and a drain region;~~

~~a second insulation film formed on the second substrate;~~

~~a trap layer continuously formed on the second insulation film;~~

~~a third insulation film formed on the trap layer;~~

a lower gate continuously formed on the trap layer, wherein the gate electrode includes ~~third insulation film;~~

~~a fourth insulation film formed on the lower gate;~~

at least two upper gates formed on ~~the fourth~~ an insulation film to be separated from each other by [[an]] the interval ~~such that at least one quantum dot can be formed in a same interval in the channel region~~.

23. (Currently Amended) The single electron transistor as claimed in claim 22, wherein the ~~first through the fourth~~ insulation ~~films are~~ is an oxide ~~films~~ film.

24. (Original) The single electron transistor as claimed in claim 22, wherein the trap layer is a nitride layer or a ferro-dielectric layer.

25. (Original) The single electron transistor as claimed in claim 22, wherein the trap layer is a layer selected from the group consisting of conductive material layers including conductive silicon layers and conductive germanium layers.

26. (Currently Amended) [[A]] The single electron transistor as claimed in claim 19, further comprising:

~~a first substrate;~~

~~a first insulation film stacked on the first substrate;~~

~~a second substrate stacked on the first insulation film and including a source region, a channel region, and a drain region;~~

~~a second insulation film formed on the second substrate;~~

~~at least two trap layer patterns having a separation distance therebetween formed on the second insulation film and in a third insulation film such that the third insulation film surrounds the at least two trap layer patterns on all surfaces except bottom surfaces thereof which contact the second insulation film;~~

a lower gate continuously formed on the ~~third~~ insulation film; and

~~a fourth~~ another insulation film formed on the lower gate [[;]], wherein the gate electrode includes at least two upper gates formed on the ~~fourth~~ another insulation film to be aligned with the at least two trap sections ~~layer patterns~~, and to be separated from each other by [[an]] the interval ~~such that at least one quantum dot can be formed in a same interval in the channel region, the interval corresponding to the separation distance between the at least two trap layer patterns~~.

27. (Currently Amended) The single electron transistor as claimed in claim 26, wherein the at least two trap sections ~~layer patterns~~ are formed of a material selected from the group consisting of conductive materials including conductive silicon and conductive germanium.

28. (Currently Amended) The single electron transistor as claimed in claim 26, wherein the trap sections ~~layer patterns~~ are formed of a nitride or a ferro-dielectric.

Claims 29-43. (Canceled).

44. (New) A single electron transistor having a memory function, comprising:

a substrate including a source region, a channel region, and a drain region;

a trap layer formed on the substrate; and

a gate electrode opposite the trap layer, wherein at least one of the gate electrode and the trap layer has an interval therein such that at least one quantum dot can be formed in a same interval in the channel region.

45. (New) The single electron transistor as claimed in claim 44, further comprising a tunneling film formed between the substrate and the trap layer.

46. (New) The single electron transistor as claimed in claim 44, wherein a size of the at least one quantum dot is 100 nm or less at room temperature.

47. (New) The single electron transistor as claimed in claim 44, wherein the trap layer is a nitride layer or a ferro-dielectric layer.

48. (New) The single electron transistor as claimed in claim 44, wherein the trap layer is selected from the group consisting of conductive material layers including a conductive silicon layer and a conductive germanium layer.

49. (New) The single electron transistor as claimed in claim 44, wherein the interval includes at least two intervals such that at least one quantum dot can be formed in a same interval for each of the at least two intervals in the channel region.

50. (New) The single electron transistor as claimed in claim 49, wherein the at least two intervals have different widths.

51. (New) The single electron transistor as claimed in claim 1, wherein the gate electrode extends on and between the trap sections.

52. (New) The single electron transistor as claimed in claim 1, wherein the tunneling film extends between the trap sections.

53. (New) The single electron transistor as claimed in claim 1, wherein the tunneling film is on and between the trap sections.

54. (New) The single electron transistor as claimed in claim 1, wherein the tunneling film completely surrounds the trap sections.

55. (New) The single electron transistor as claimed in claim 17, further comprising another insulation film formed on and between the conductive spacers.